REMARKS

In the Official Action mailed 12 January 2005, the Examiner reviewed claims 1-65. The Examiner rejected claims 1-65 under 35 U.S.C. §103(a).

No claims are amended. Claims 1-65 remain pending.

The Examiner's rejection is respectfully traversed below.

Rejection of Claims 1-65 under 35 U.S.C. §103(a)

Claims 1-65 are rejected under 35 U.S.C. §103(a) as being unpatentable over Walukas, 6,229,737, in view of Lin *et al.*, 6,671,209. Reconsideration is respectfully requested. To present a *prima facie* case, the Examiner must identify each of the claim limitations in a combination of references cited, as well as provide a reasonable basis for a motivation to combine the references with a reasonable likelihood of success. Applicant submits that in the present official action, the Examiner has not met the first requirement of the *prima facie* case, because Examiner has not identified each of the claim limitations in a combination of references. *A priori*, the Examiner has not provided any basis for the second and third requirements of the *prima facie* case as to the missing limitations.

In particular, the Examiner has overlooked limitations in each of the independent claims 1, 23, 46 in the present application, which require that the "first memory array" and the "second memory array" are formed on a single integrated circuit. For example, claim 1 includes the limitations "a first memory array on the substrate..." and "a second memory array on the substrate..." The "substrate" in claim 1 is a semiconductor substrate. Walukas discloses a memory system that comprises two separate semiconductor devices (E^2ROM 12 and FLASH 14 in Fig. 1), presumably mounted on a circuit board. The E^2PROM and FLASH devices relied upon by the Examiner are separate integrated circuits altogether. In fact, at Walukas, column 3, line 49-55, the embodiment described comprises a first device manufactured by Atmel (AT28HC256), and a second device manufactured by AMD (AM29F040). Thus, rather than two arrays on a single die as claimed herein, Walukas describes two devices made by different manufacturers altogether. There is no description in Walukas of a single semiconductor substrate having first and second memory arrays thereon.

The Examiner relies on Lin *et al.* to suggest specific memory cell structures and programming operations. However, Lin *et al.* does not teach using different operation

algorithms for arrays on a single chip, and otherwise does not overcome the deficiencies of the Examiner's *prima facie* case.

Therefore, the *prima facie* case presented by the Examiner is incomplete, and reconsideration of the rejection is requested on that basis.

As explained in the specification of the present application, it is desirable to form two memory arrays on a single die and operate them differently to support modes of operation that are adapted for storing code and for storing data. See application as filed, page 3, lines 9-12, page 6, lines 21-30. The prior art as represented by Walukas utilizes separate integrated circuits to support the different modes of operation.

Claims 2-22 depend from claim 1, and are allowable for at least the same reasons, and because of the unique combinations recited. In addition, the Examiner did not make supporting citations to the references with respect to any of the dependent claims. For example, claim 3 states that both the first and second memory arrays comprise charge trapping memory cells. Accordingly, claim 3 requires that two memory arrays of charge trapping memory cells on a single substrate be operated in different modes. The references applied by the Examiner do not suggest this limitation.

Claim 23 recites a method for manufacturing a device, including forming both the first and the second arrays on a single semiconductor substrate. The Examiner did not specifically mention claim 23 in the Official Action. Nonetheless, the references applied by the Examiner do not suggest this manufacturing method. The E^2PROM and FLASH devices relied upon by the Examiner are separated integrated circuits altogether. Claims 24-45 depend from claim 23 and are patentable for at least the same reasons, and because of unique combinations recited

Claim 46 recites the method for operating an integrated circuit, which requires addressing first and second memory arrays on a single integrated circuit, and reading, programming and erasing data in one of the arrays according to an operation algorithm, while reading, programming and erasing code in other of the arrays according to a different operation algorithm. The references relied upon by the Examiner illustrate that the prior art has relied upon separate integrated circuits for the purposes of handling the code and data modes of operation. Claims 47-65 depend from claim 46, and are patentable for at least the same reasons, and because of the unique combinations recited.

The present inventors have proposed one integrated circuit device with memory cells on the device arranged into two memory arrays, and wherein the two memory arrays are operated using different operation algorithms. The claims herein are directed to the structure, the method for manufacturing and the method for operating such device. Applicant submits that the Examiner has not presented a *prima facie* case that supports all the limitations in the independent claims.

Furthermore, the inventors have suggested that the two memory arrays could be manufactured with memory cells that are substantially the same in both arrays, as stated in a number of the dependent claims. Using substantially the same memory cells for two different memory arrays on a single integrated circuit, and operating the two memory arrays differently is not suggested by any of the references relied upon by the Examiner.

Accordingly, reconsideration of the rejection of claims 1-65 as amended is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1571-1).

Respectfully submitted,

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